

Monolithic Amplifier

50Ω, Broadband, DC to 4 GHz

NEW!
ERA-5XSM



CASE STYLE : WW107

Features

- wide bandwidth, DC-4 GHz
- high gain, 20.5 dB typ. at 100 MHz
- high dynamic range, 3.5 dB NF, 33 dBm IP3
- low thermal resistance for high reliability
- built in transient protection
- patent pending

Applications

- cellular
- PCS
- communication receivers & transmitters

Electrical Specifications @ 25°C

MODEL NO.	FREQ.* (GHz)	GAIN, dB Typical					MAXIMUM POWER (dBm) @ 1 GHz Output (1dB Comp.) Typ. Input (no dmg.) Min.			DYNAMIC RANGE @ 1 GHz NF (dB) Typ. IP3 (dBm) Typ.		VSWR (:1) Typ. In DC-3 GHz Out 3-4 GHz DC-3 GHz 3-4 GHz				MAXIMUM RATING** I P mA mW		DC OPERATING POWER @ Pin 3*** Current (mA) Typ Volt Min Max				THERMAL RESISTANCE θjc, typ. °C/W	PRICE \$ Qty. (25)	
		0.1	1	2	3	4	Min. @ 2 GHz	Typ.	Min.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	
ERA-5XSM	DC-4	20.5	19.5	17.6	15.5	13.7	16	17.8	16.5	13	3.5	33	1.2	1.3	1.2	1.4	120	650	65	4.9	4.2	5.5	133	1.69

* Low frequency cutoff determined by external coupling capacitors.

** Permanent damage may occur if any of these limits are exceeded.

These ratings are not intended for continuous normal operation.

***Reliability predictions and normal operating conditions are applicable at current specified.

Maximum Ratings

Operating Temperature -45°C to 85°C

Storage Temperature -65°C to 150°C

Pin Configuration

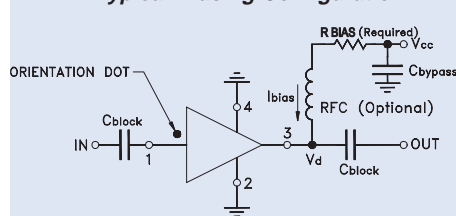
RF IN	1
RF OUT	3
DC	3
GND EXT.	2,4

Model Identification

Model	Marking†
ERA-5XSM	5X

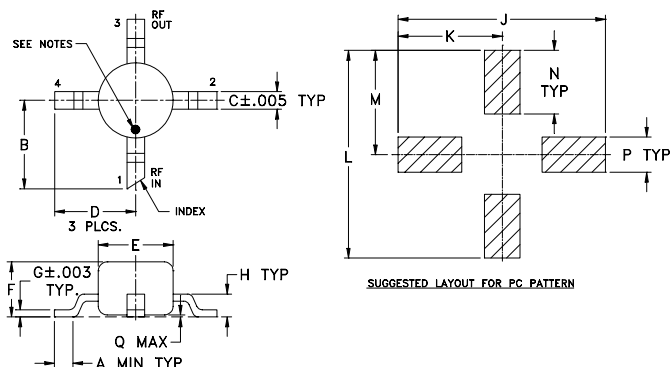
† Prefix letter (optional) designates assembly location. Suffix letters (optional) are for wafer identification.

Typical Biasing Configuration



R BIAS "1%" Resistor Values	
Vcc	ERA-5XSM
7	33.2
8	48.7
9	63.4
10	78.7
11	95.3
12	110
13	124
14	140
15	158
16	174
17	187
18	205
19	221
20	232

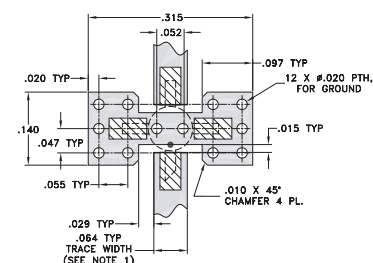
Outline Drawing



Outline Dimensions (inch mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	wt. grams
.012	.10	.020	.092	.085	.060	.007	.026	.235	.118	.235	.118	.072	.040	.020	.015
.30	2.54	.51	2.34	2.16	1.52	.18	.66	5.97	3.00	5.97	3.00	1.83	1.02	0.51	

Suggested PCB Layout (PL-075)



NOTES:

1. TRACE WIDTH IS SHOWN FOR ROGERS RO4350 WITH DIELECTRIC THICKNESS 0.030" ± 0.002", COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. IF YOUR PCB DESIGN RULES ALLOW, GROUND VIAS SHOULD BE PLACED UNDER THE LAND PATTERN FOR BETTER RF PERFORMANCE. OTHERWISE GROUND VIAS SHOULD BE PLACED AS CLOSE TO LAND PATTERN AS POSSIBLE.

- DENOTES PCB COPPER LAYOUT
- DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK



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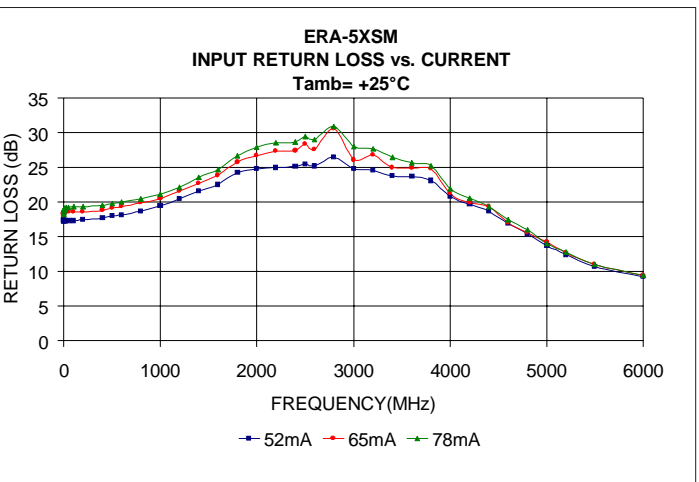
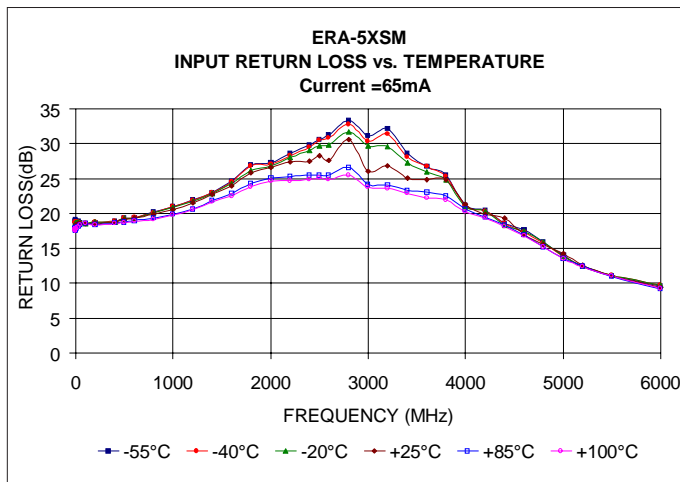
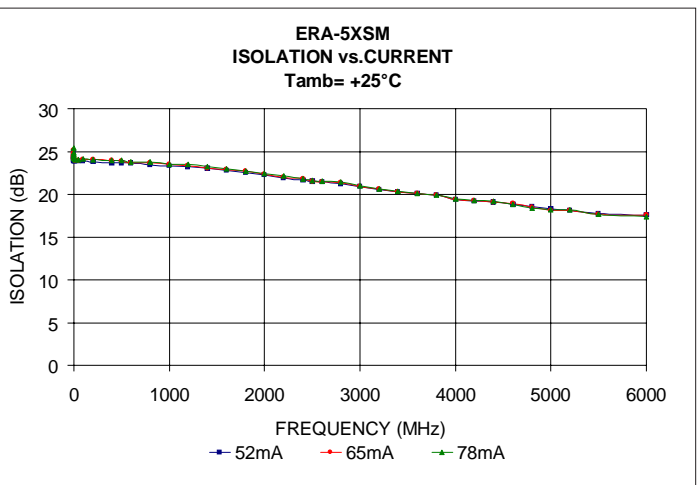
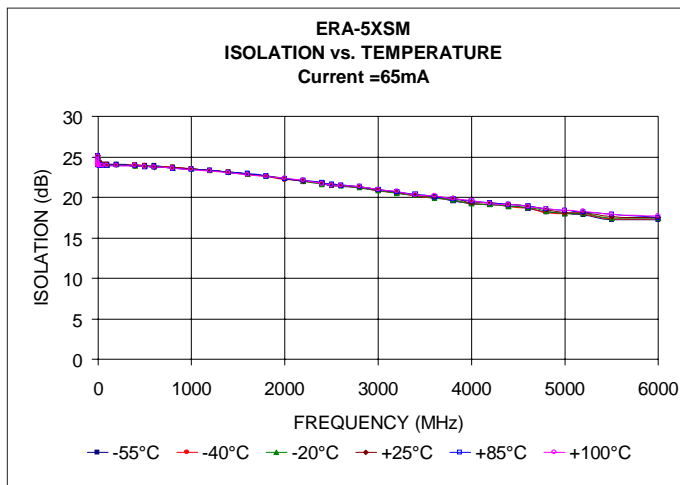
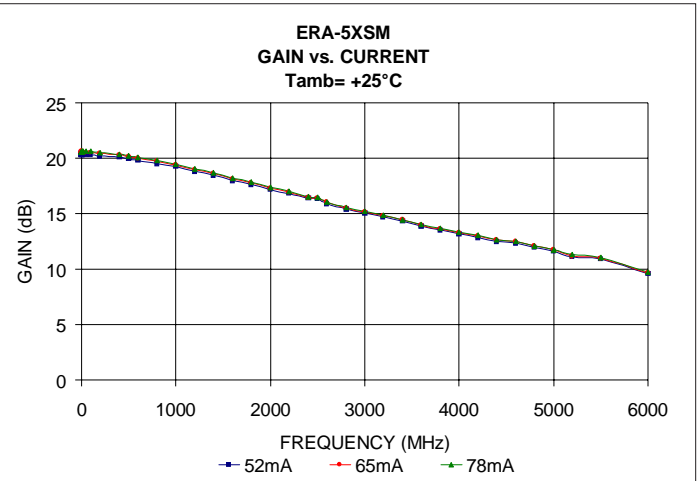
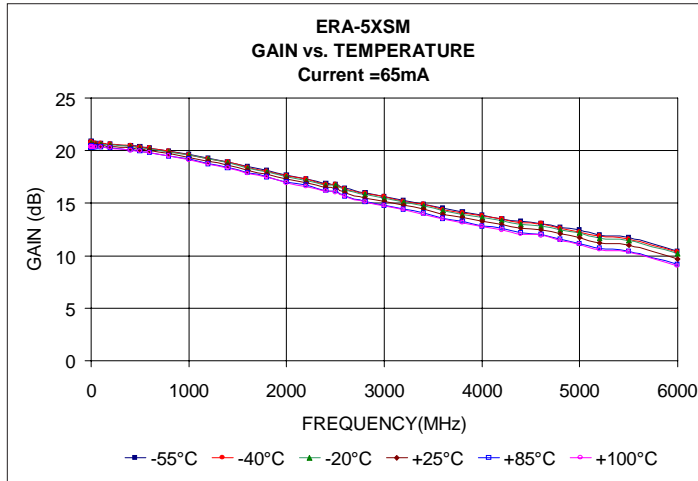
ISO 9001 CERTIFIED

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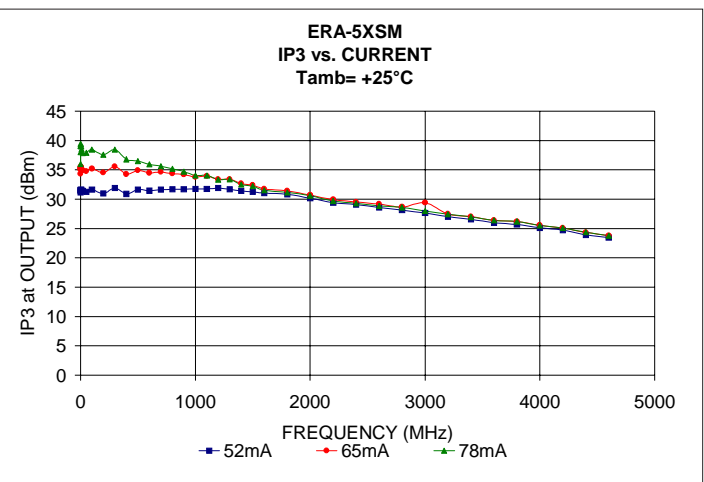
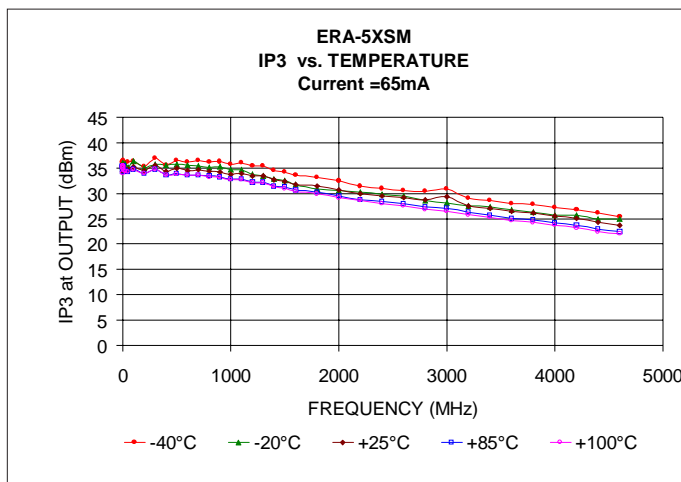
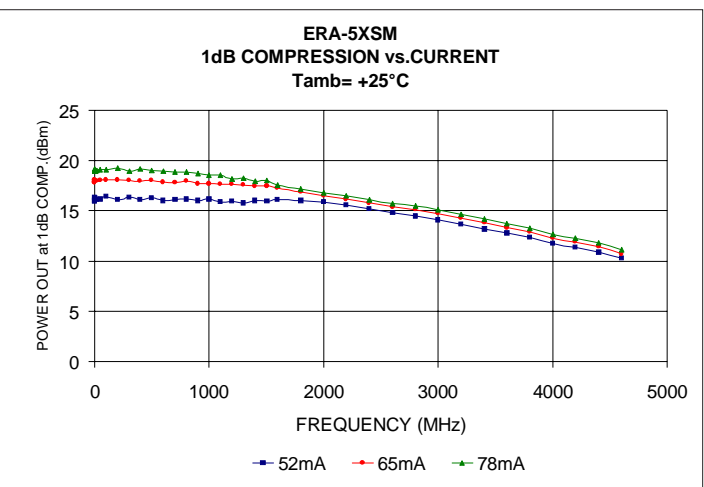
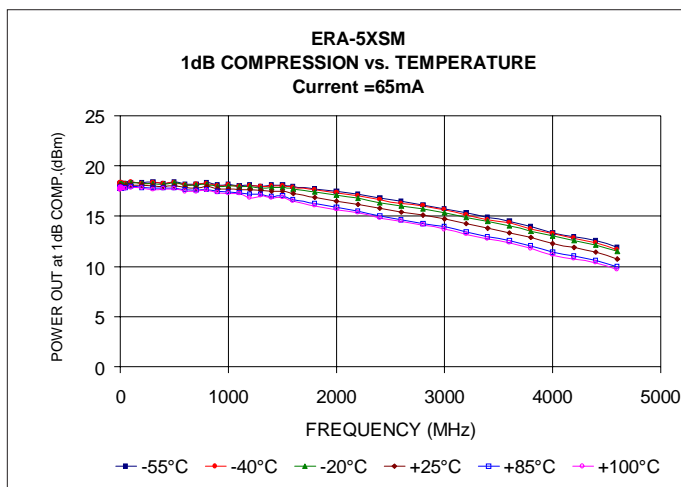
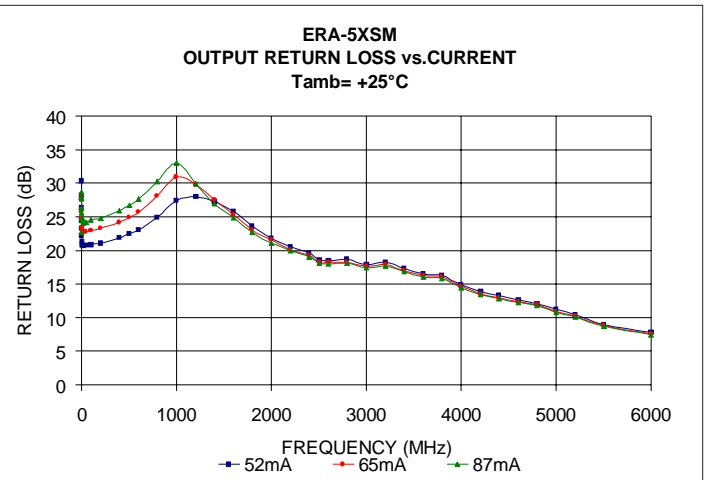
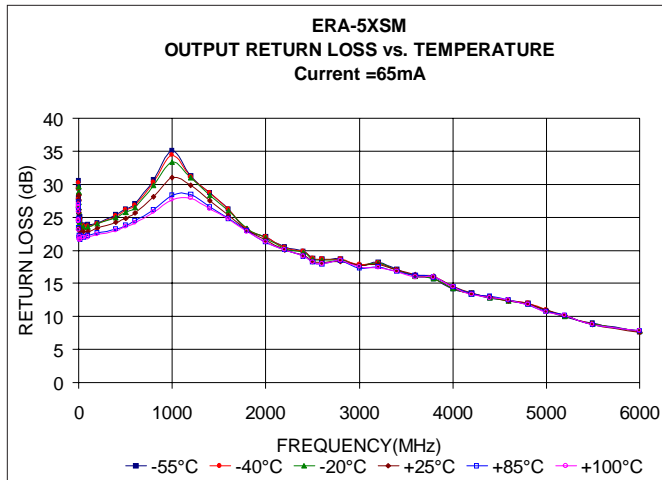
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Performance Curves



Performance Curves



Performance Curves

